EUVL & 450mm HVM
The Intersection Point?

Panel Discussion
2013 International Workshop on EUV Lithography
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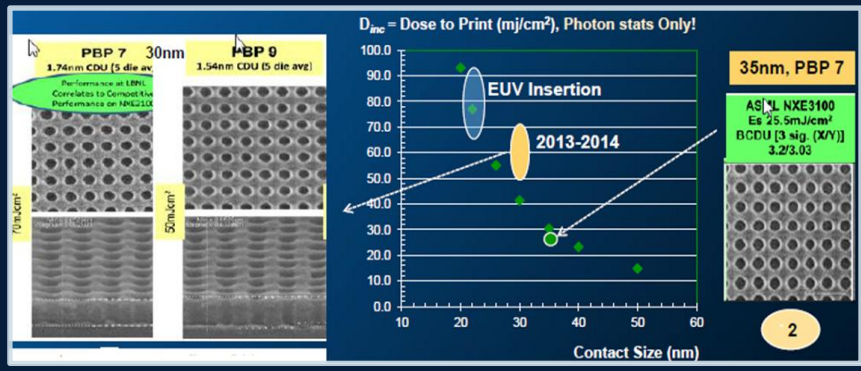
2012 Panel Discussion Summary

EUV HVM Characterizations

(Yan B, Intel)

1. Edge Placement Error Challenges for Multiple Patterning
2. EUV Photon Noise ➔Potentially Higher Source Power Requirements.
3. OPC Requirements for EUV HVM



Mask Related Issues

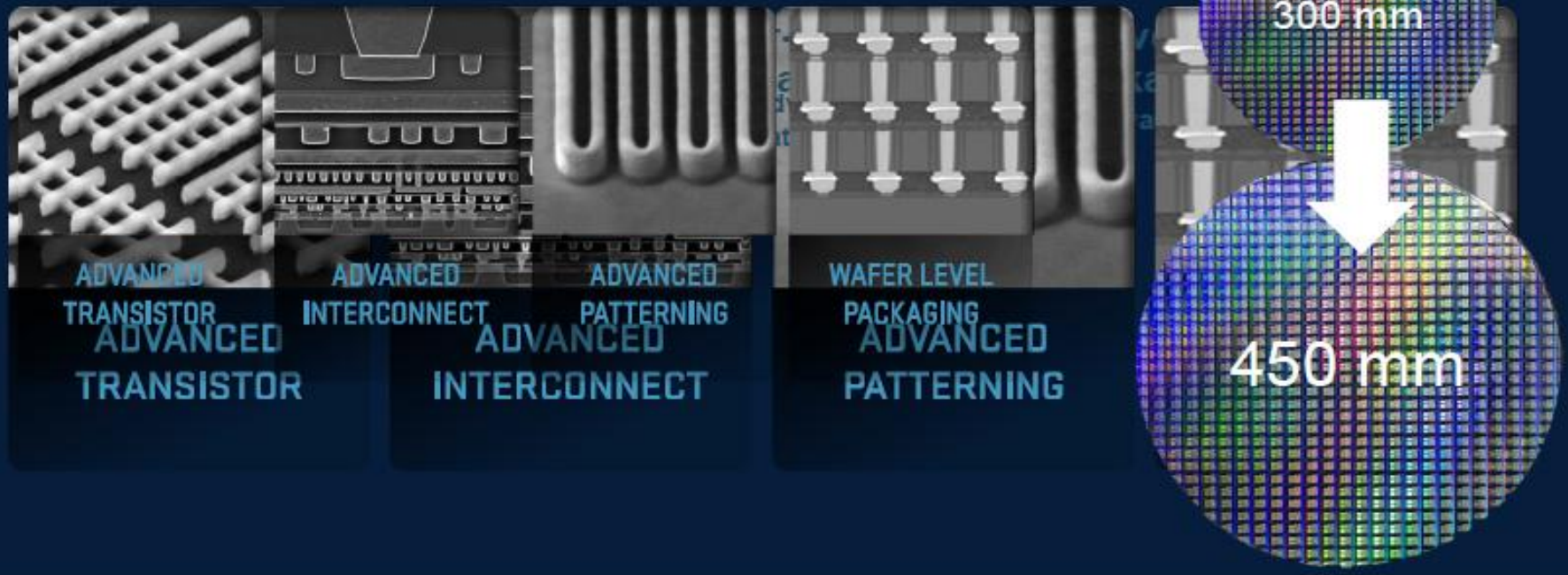
(Pawitter M, Global Foundries & Takashi San, Toshiba Corp)

1. AIMS (printability checks) Delays Would Require E-beam and Simulation Based Mask Defect Detection Alternatives.
2. 2017 = Earliest Possible EUV HVM Insertion Timeframe with Significant EUVL Productivity Improvements Required.
3. Mask R&D Requirements Highlighted for High NA (>0.4) and for BEUV (6.x) Wavelengths.

Ramp of Complexity in the next 5 years

EUV, E-Beam Inspection, III-V Materials
3-D NAND, Integrated Processing,
Material Modifications
Conformal Films, Hi-K ALD

PVD → Metal CVD, Flowable Films
Quad patterning, High Aspect Ratio Tech
Sacrificial Films, Complementary p
Lamp Based Processing, TSV



R&D of 450mm needed in parallel to all 300mm technology inflections

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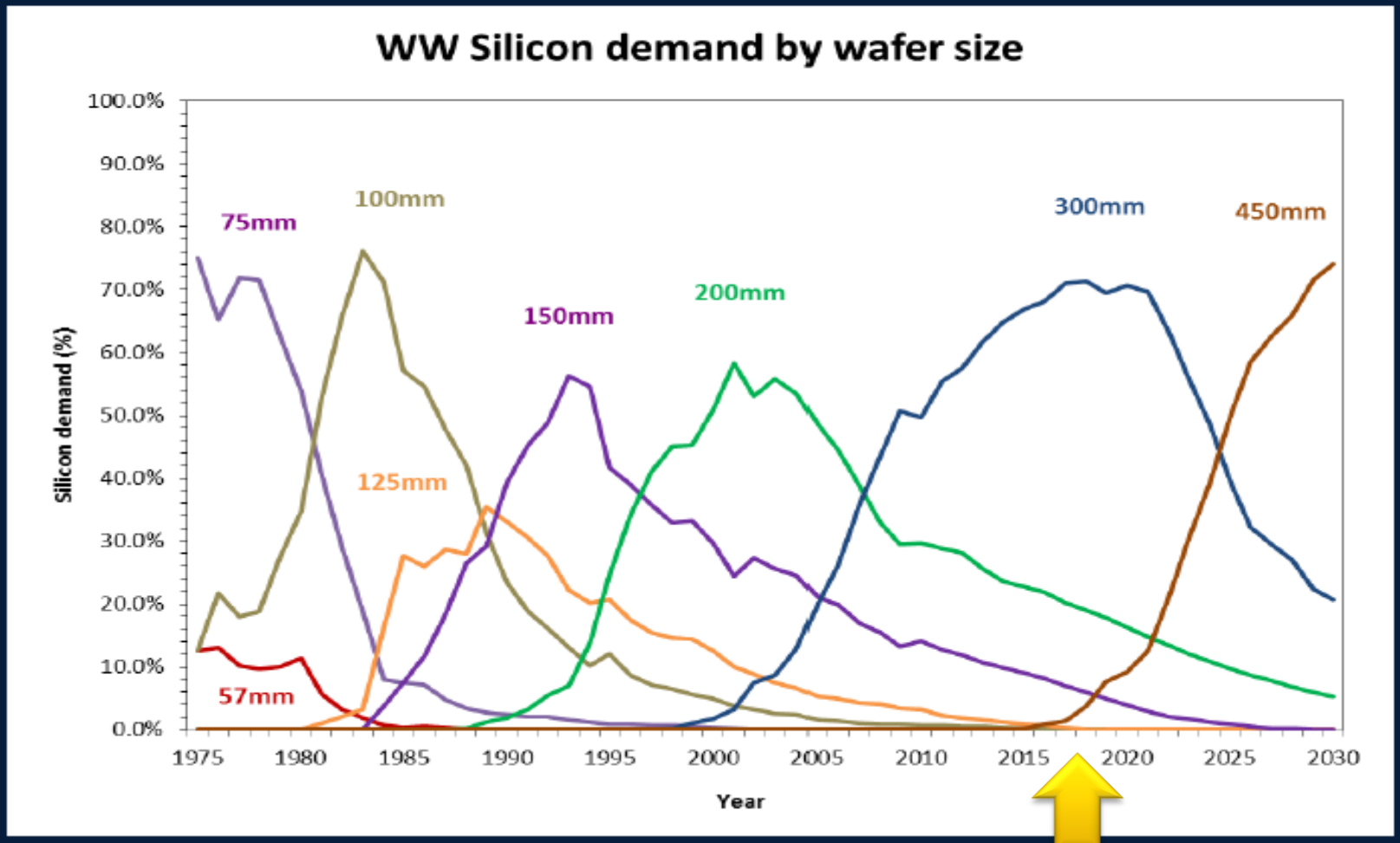
Silicon Demand by Wafer Size



Projected 450mm Ramp Rate. Assumptions?

Ack: IC Insights

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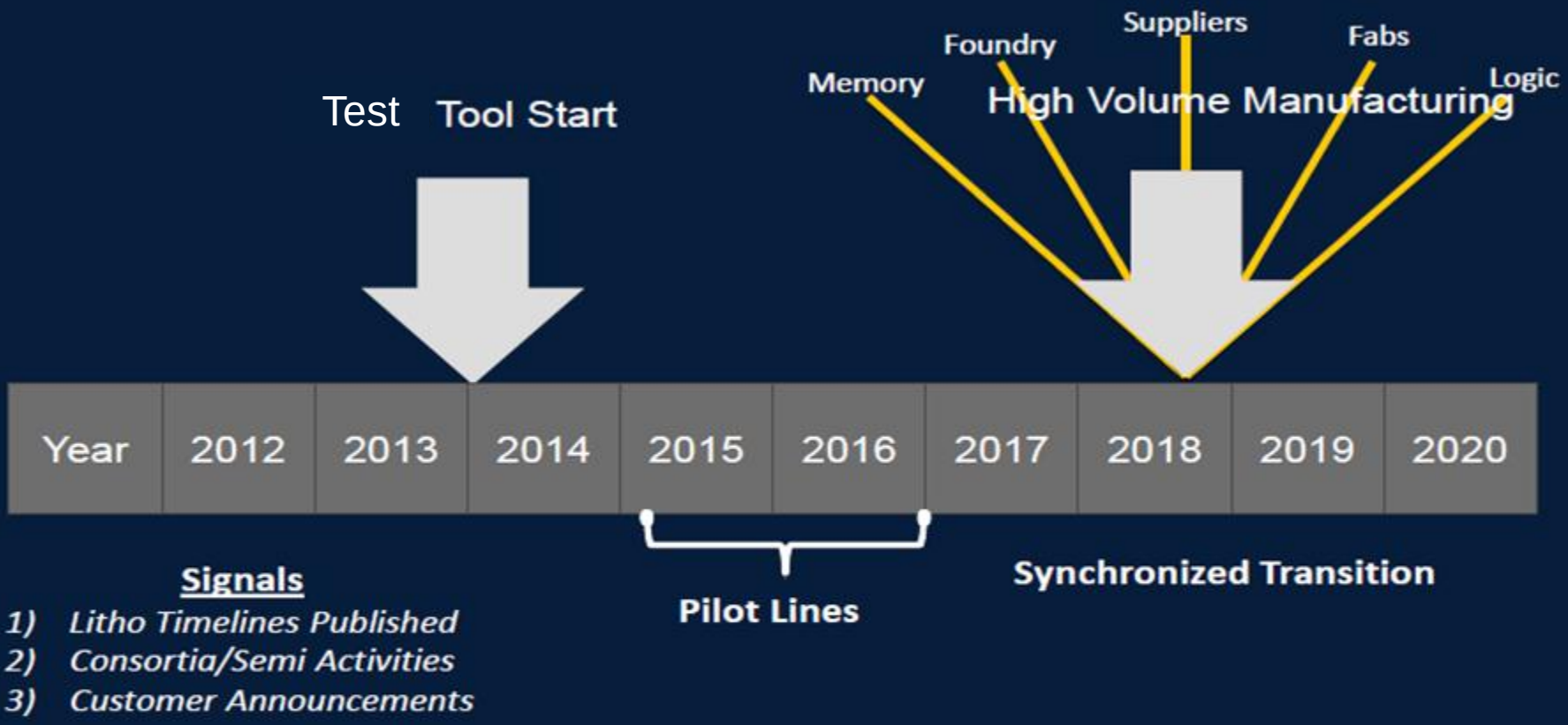
450mm HVM

Key Factor # 1, Lithography/Patterning Solutions for sub10nm

Key Factor # 2, Synchronized Timelines



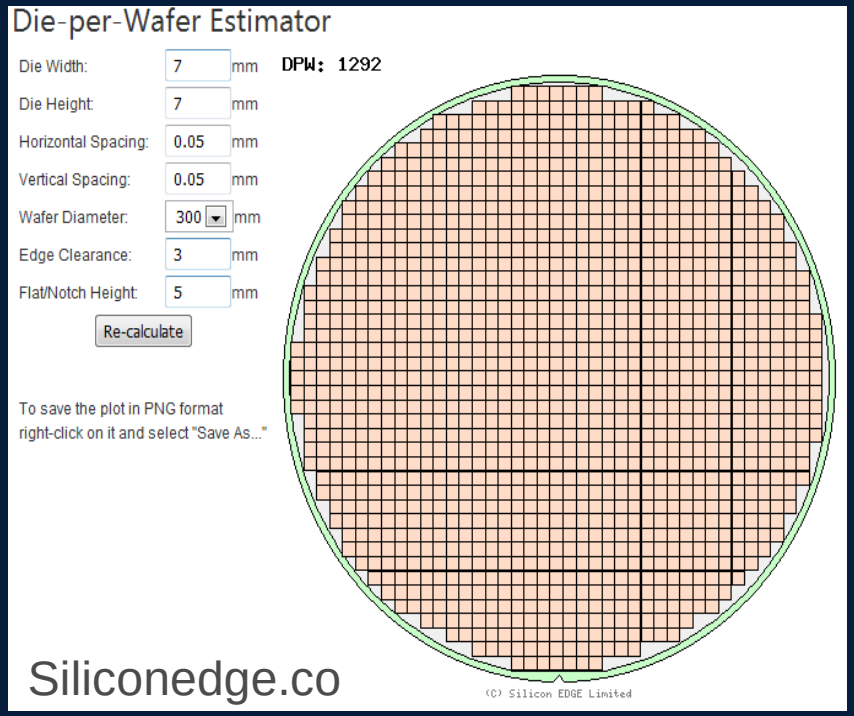
Synchronized Timelines lowers the overall cost of Transition

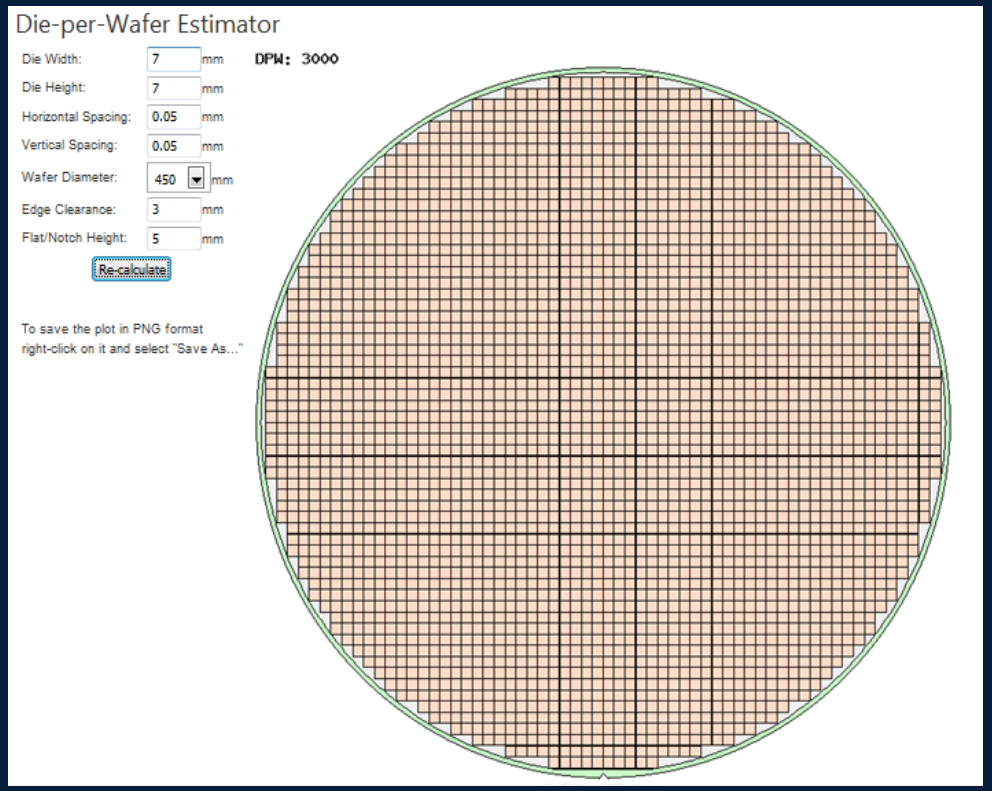
Wafer Size Transition: Performance vs. TPT vs. Cost

Die-Maps (~50mm2 die for low power IC's)

300mm: 1292 Die
Outer 10mm
Wafer Area ~180die

450mm: 3000 Die
Outer 10mm
Wafer Area ~280die

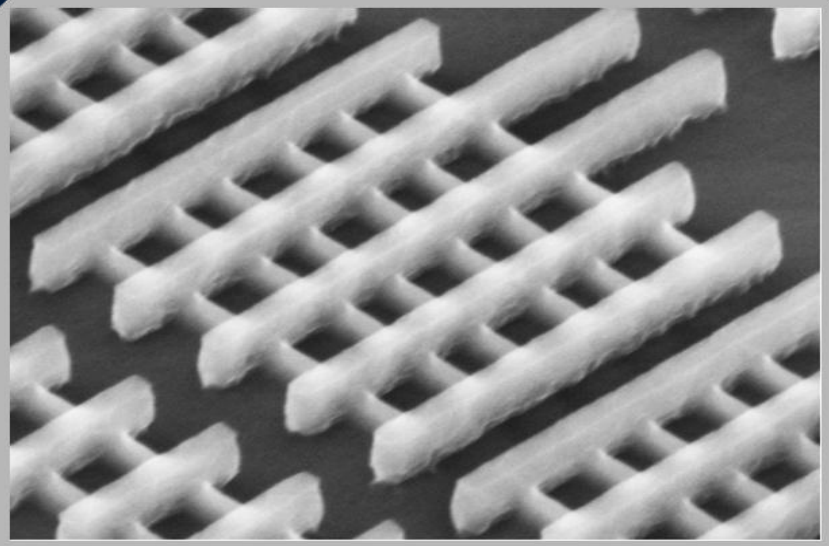




450mm Challenges

- **Chamber Technologies: Edge Process Control**
- **Beam Tools (implant, photon scan tools): TPT/Wfr~0.5x 300mm**

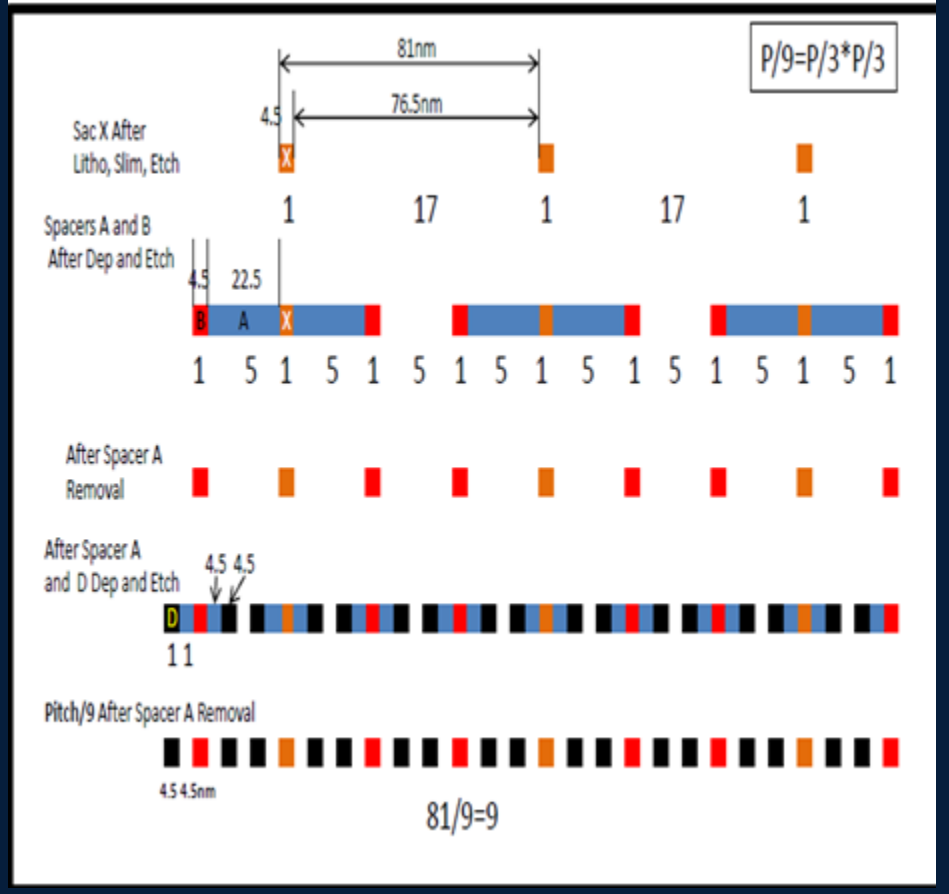
450mm: EUV or 193i Multi-Patterning



Courtesy: C-H-Jan Et, Al, Intel, IEDM 2012

- 2xnm SRAM Layouts
  - Scale to 5nm with 193i MP?

Double – Quad – Hexa – Nona Patterning



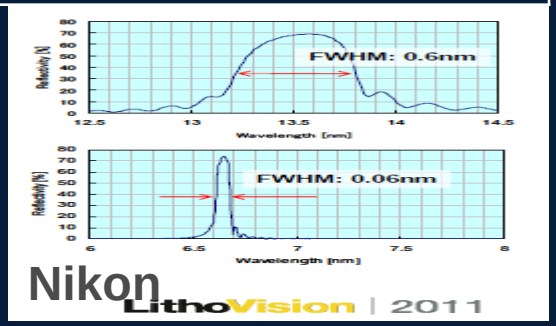
Courtesy: Yan B/Intel, VLSI, 2012

193i Multi-patterning Could Enable 7nm/5nm Devices
What costs will this entail?

EUVL 5-7nm ITRS Node Scaling Paths (2017-2020)

EUV Scaling Paths	Issues/Challenges
8-12nm HP Patterning Paths with EUVL for 2017-2020	
13.5nm Double Patterning, Lower K1	**193nm Like RET (ePSM,aPSM?),COO**
13.5nm >0.5 "Hyper NA"	**Power Loss**
6.8nm Beyond EUV (Soft X-rays)	**Time, New Infrastructure**

	Source	Mirrors	Peak R%
13.5nm	**Sn**	Mo/Si/B4C	>70%
6.Xnm	**Tb/Gad**	LaN/B4C	Empirical 50%?
Smaller Spectral band-Width, Increased Interface Complexity, New Emission Sources.			



Best Guess 5-7nm Litho Solutions

- 13.5nm EUV/SADP
- "193i Multi-patterning + 13.5nm EUV"

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Summary

450mm EUV Insertion

Engineering challenges with chamber technologies on similar scale as beam tool TPT scaling (litho source power, implant etc).

- + AMAT is solving the chamber engineering issues (edge uniformity and control for example) with ingenuity
- - The cost aspects of such engineering solutions (chamber as well as beam) is to be further understood. (slide 6)

450mm Era: EUV vs. 193i.

193i multi-patterning will exist even with 450mm with EUV 450mm dependent on source power hitting >150-250W in HVM. (slide 7)

On EUV 13.5nm vs. 6.xnm in the 450mm era, the current view is that 13.5nm EUV multi-patterning would be a better choice considering the long development time taken for 13.5nm development. (slide 8)